



Europäisches Patentamt  
European Patent Office  
Office européen des brevets



Publication number:

**0 678 997 A1**

(12)

## EUROPEAN PATENT APPLICATION

(21) Application number: 95104052.6

(51) Int. Cl.<sup>6</sup>: H04L 12/56

(22) Date of filing: 20.03.95

(30) Priority: 20.04.94 GB 9407806

(43) Date of publication of application:  
25.10.95 Bulletin 95/43

(84) Designated Contracting States:  
AT BE CH DE DK ES FR IT LI SE

(71) Applicant: **ROKE MANOR RESEARCH LIMITED**  
Roke Manor  
Romsey,  
Hampshire, SO51 0ZN (GB)

(72) Inventor: **Hayter, Andrew Timothy**  
3 Cobden Gardens

**Bitterne Park,**  
**Southampton SO18 1LN (GB)**  
Inventor: **Davis, Simon Paul**  
**17 Westering**  
**Romsey,**  
**Hampshire SO51 7LX (GB)**

(74) Representative: **Allen, Derek**  
**Siemens Group Services Limited**  
**Intellectual Property Department**  
**Roke Manor**  
**Old Salisbury Lane**  
**Romsey**  
**Hampshire SO51 0ZN (GB)**

(54) Improvements in or relating to ATM communication systems.

(57) An ATM communication system having DBA, comprising storage means for DBA traffic, which storage means includes dedicated storage means for ABR traffic, the system being such that ABR bandwidth requests are allocated after all other DBA bandwidth allocations have been satisfied, means

being provided for interrupting an ABR transmission, before a bandwidth allocation within which the said ABR transmission is included has been fully used, for the transmission of other higher priority DBA traffic.

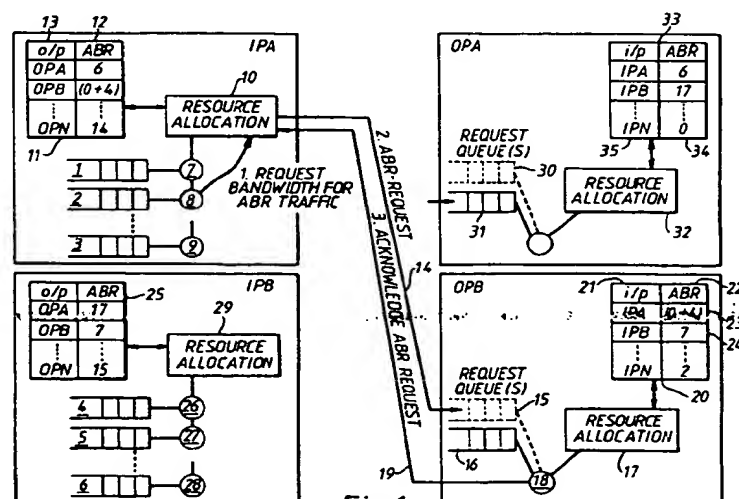


Fig. 1

EP 0 678 997 A1

This invention relates to asynchronous transfer mode (ATM) communication systems.

ATM communication systems comprise networks and switches required to support a mixture of traffic including bursty traffic. By its nature, bursty traffic requires high bit-rate transmission for a part of the time and little or no transmission for the rest of the time. In order to efficiently use the bit-rate available in a network, it is necessary to allocate to a connection a lower bit-rate than its peak bit-rate such that the total peak bit-rate of all connections is greater than the bit-rate of the network links in combination.

ATM cells destined for a particular output port of a switch, will enter the switch from many different input ports. The total instantaneous rate of these cell flows may be greater than the output port of an ATM switching network (ASN) can sustain, and thus a temporary overload of the output port may occur. Reducing the output port average load may reduce the probability of this overload to an operational acceptable level, but this results in a low utilisation of the network which is not generally acceptable.

In an alternative approach, large buffers may be included in an ATM switch which serve to buffer the overload cells causing them to be delayed so that they can be transmitted at the peak rate. One of the problems with large buffers, however, is that the transmission of ATM cells across a switch becomes very complex and requires organising in a fair manner. This problem may however be satisfactorily overcome by means of a technique known as 'Dynamic Bandwidth Allocation' (DBA) which may be used to share fairly the bandwidth available between data input queues to a switch. The operation of DBA forms the subject of and is described in our co-pending patent application number 9322744.5 to which attention is hereby directed.

Although the DBA protocol described in our co-pending patent application number 9322744.5 is satisfactory for most purposes, there is a requirement for a new service, which is characterised as being loss sensitive but delay insensitive, i.e. intolerant of cell loss but tolerant of longer than usual delays and it will hereinafter be referred to as 'Available Bit-Rate' (ABR) service. This new proposed ABR service is intended for system users which require to move data around but do not mind how long it takes. The ABR service is also useful for network operators because it may be implemented by buffering data at the ingress of a switch and only sending it across a switch core when bandwidth is not being used for any other services, which thus increases network utilisation and profitability. It would be desirable to provide a system having both DBA and ABR but known DBA sys-

tems do not facilitate this.

It is therefore an important object of the present invention to provide an ATM communication system having DBA, which will also provide for ABR service traffic.

It is probably worth mentioning at this juncture that methods of stopping data arriving at an ingress of a switch, such that ingress buffers are not caused to overflow, is a separate problem which will not hereinafter be addressed.

According to the present invention, an ATM communication system having DBA, comprises storage means for DBA traffic, which storage means includes dedicated storage means for ABR traffic, the system being such that ABR bandwidth requests are allocated after all other DBA bandwidth allocations have been satisfied, means being provided for interrupting an ABR transmission, before a bandwidth allocation within which the said ABR transmission is included has been fully used, for the transmission of other (higher priority) DBA traffic.

The ATM communication system may comprise a plurality of statistical multiplexer units (SMU's) on an 'input side' of the switch and a plurality of SMU's on an 'output side' of the switch, the 'input side' SMU's comprising a plurality of stores, one for each 'output side' SMU, in which ATM cells for transmission across the switch are stored, each store on the 'input side' of the switch being operatively associated with a server, the servers being controlled in accordance with the DBA protocol by 'input side' resource allocation means, so as to effect transmission as aforesaid in a fair manner.

The resource allocation means may include a RAM table for storing data appertaining to the bandwidth or bit rate allocated to ABR traffic to each of the 'output side' SMU's.

Each SMU on the 'output side' of the switch may include an ABR request store which forms a part of 'output side' resource allocation means, within which ABR request store, ABR bandwidth requests are stored, the 'output side' resource allocation means being arranged to provide acknowledgement signals indicative of resource availability, which acknowledgement signals are transmitted across the switch to the 'input side' resource allocation means so as appropriately to initiate data transmission across the switch.

It is important to appreciate that these acknowledgement signals not only indicate in respect of each 'output side' SMU when ABR bandwidth has become available, but also when allocated ABR bandwidth should be withdrawn for the time being, thereby to make available bandwidth for other (higher priority) DBA traffic.

It should be understood that DBA bandwidth resource requests and acknowledgement signals are transmitted across the switch to facilitate normal DBA operation and that dedicated ABR requests and acknowledgements are additionally transmitted and stored as appropriate. It is therefore necessary in each 'output side' SMU to provide storage means in which ABR bandwidth requests are stored separately from all other DBA bandwidth requests. In this way bandwidth resource allocation can be managed efficiently such that ABR, ATM cells are transmitted only when all other DBA ATM cell traffic has been catered for.

One embodiment of the invention will now be described by way of example only, with reference to the accompanying drawings, in which:

FIGURE 1 is a generally schematic block diagram of a part of an ATM system showing how ABR requests and acknowledgements are transmitted across a switch; and

FIGURE 2 is a generally schematic block diagram showing 'clear-down' operation of the system shown in Figure 1, wherein appropriate parts bear the same numerical designations.

Referring now to Figure 1, an ATM system comprises a plurality of statistical multiplexing units (SMU's), only two of which, IPA and IPB are shown. The SMU's such as IPA and IPB on the 'input side' of a switch (not shown) are arranged in communication across the switch with a plurality of SMU's on the 'output side' only two of which designated OPA and OPB respectively are shown. It will be appreciated that although only two SMU's are shown on the 'input side' and 'output side' respectively of the switch, larger numbers of SMU's will be provided in accordance with the size of an installation. Within each SMU a plurality of stores are provided, within which stores ATM cells for transmission across the switch are stored. Thus in the SMU IPA, stores 1, 2 and 3 are shown and similarly in SMU IPB stores 4, 5 and 6 are shown, each 'input side' SMU having a dedicated store for each SMU on the 'output side' of the switch. Requests are triggered from the stores 1, 2 and 3 and are fed via servers 7, 8 and 9 respectively to a resource allocator 10 which comprises a RAM table of bandwidth availability on the 'output side' of the switch. The resource allocator 10 is also provided with information appertaining to the class of service to which particular ATM cells relate. Thus priority, bandwidth resource allocation becomes possible.

The parts of the system thus far described are common to a DBA system of the kind described in our co-pending GB patent application as referred to above. In order, however, to provide for an ABR service the resource allocation unit 10 is arranged additionally to include a RAM table 11 which includes data appertaining to the number, as shown

in column 12, of ABR bandwidth units for transmission and as shown in column 13 their destination on the 'output side' of the switch. Thus as can be seen from the RAM table 11, that the SMU, OPA on the 'output side' of the switch has an ABR bandwidth allocation of six bandwidth units; the SMU, OPB has requested four bandwidth units; and been granted zero bandwidth units and the SMU OPN has been granted a bandwidth allocation of fourteen bandwidth units.

As shown schematically, ABR bandwidth requests for transmission from IPA to OPB are fed via a line 14 and queued in a store 15 in the SMU OPB. Other higher priority DBA bandwidth requests are queued in a store 16. When bandwidth is available, as determined by a resource allocator 17, acknowledgements are sent via a server 18 and a line 19 to the resource allocator 10 in the SMU IPA. The resource allocator 17 includes a dedicated RAM table 20 for ABR messages which is additional to RAM storage (not shown in detail) for the other DBA bandwidth requests. Bandwidth requests appertaining to the input SMU's are designated in column 21 and bandwidth units appertaining to each SMU listed is as shown in column 22. Thus it can be seen that the SMU IPA has requested four units of bandwidth but has so far received a zero allocation. Similarly it can be seen that the input SMU IPB has been allocated seven units of bandwidth. This corresponds to the contents of RAM table 25 in the SMU IPB. It will be appreciated that the stores 4, 5 and 6 in the SMU IPB communicate via servers 26, 27 and 28 under control of a resource allocator 29 with SMU's on the 'output side' of the switch. It will also be appreciated that the SMU OPA on the 'output side' of the switch is provided with a store 30 for ABR requests and a store 31 for other DBA requests, the stores 30 and 31, which correspond with the stores 15 and 16 respectively of the SMU OPB and are operated under control of a server 32a corresponding to the server 18. Similarly a resource allocator 32b is provided in the SMU OPA which includes a RAM table 33 shown in detail, in which are stored details of the number of units of bandwidth allocated as shown in a column 34 and the input SMU's to which they relate as shown in a column 35, the server 32a being controlled by the resource allocator 32b.

It is important to appreciate that allocated ABR bandwidth can be cleared down to facilitate the transmission of higher priority DBA traffic and the manner in which this is effected is shown schematically in Figure 2 wherein corresponding parts of the system bear, where appropriate, the same numerical designations.

Referring now to Figure 2, as shown schematically by means of a line 36, clear-down requests

are routed to all resource allocators that have acting ABR traffic on OPB including the resource allocator 10 from the server 18 when bandwidth is required by the SMU OPB for non ABR traffic, whereby the transmission of ABR traffic is temporarily decreased in rate. Similarly clear-down signals are sent as appropriate from the server 18 via a line 37 to the resource allocator 28 for a similar purpose as required by the SMU IPB.

Various modifications may be made to the arrangements shown without departing from the scope of the invention and, for example, any number of SMU's may be provided on the input of a switch with a corresponding number on the 'output side' of the switch in accordance with the size of the system.

### Claims

1. An ATM communication system having DBA, comprising storage means for DBA traffic, which storage means includes dedicated storage means for ABR traffic, the system being such that ABR bandwidth requests are allocated after all other DBA bandwidth allocations have been satisfied, means being provided for interrupting an ABR transmission, before a bandwidth allocation within which the said ABR transmission is included has been fully used, for the transmission of other higher priority DBA traffic.
2. An ATM communication system as claimed in Claim 1, comprising a plurality of statistical multiplexer units (SMU's) on an 'input side' of the switch and a plurality of SMU's on an 'output side' of the switch, the 'input side' SMU's comprising a plurality of stores, one for each 'output side' SMU, in which ATM cells for transmission across the switch are stored, each store on the 'input side' of the switch being operatively associated with a server, the servers being controlled in accordance with a DBA protocol by 'input side' resource allocation means.
3. An ATM communication system as claimed in Claim 2, wherein the resource allocation means includes a RAM table for storing data appertaining to the bit rate or bandwidth allocated to ABR traffic for transmission to each of the 'output side' SMU's.
4. An ATM communication system as claimed in Claim 3, wherein each SMU on the 'output side' of the switch includes an ABR request store which forms a part of 'output side' resource allocation means, within which ABR re-

quest store, ABR bandwidth requests are stored, the 'output side' resource allocation means being arranged to provide acknowledgement signals indicative of resource availability, which acknowledgement signals are transmitted across the switch to the 'input side' resource allocation means so as appropriately to initiate data transmission across the switch.

5. An ATM communication system as claimed in Claim 4, wherein the acknowledgement signals are arranged to indicate in respect of each 'output side' SMU when ABR bandwidth has become available and also when allocated ABR bandwidth should be withdrawn for the time being, thereby to make available bandwidth for other higher priority DBA traffic.

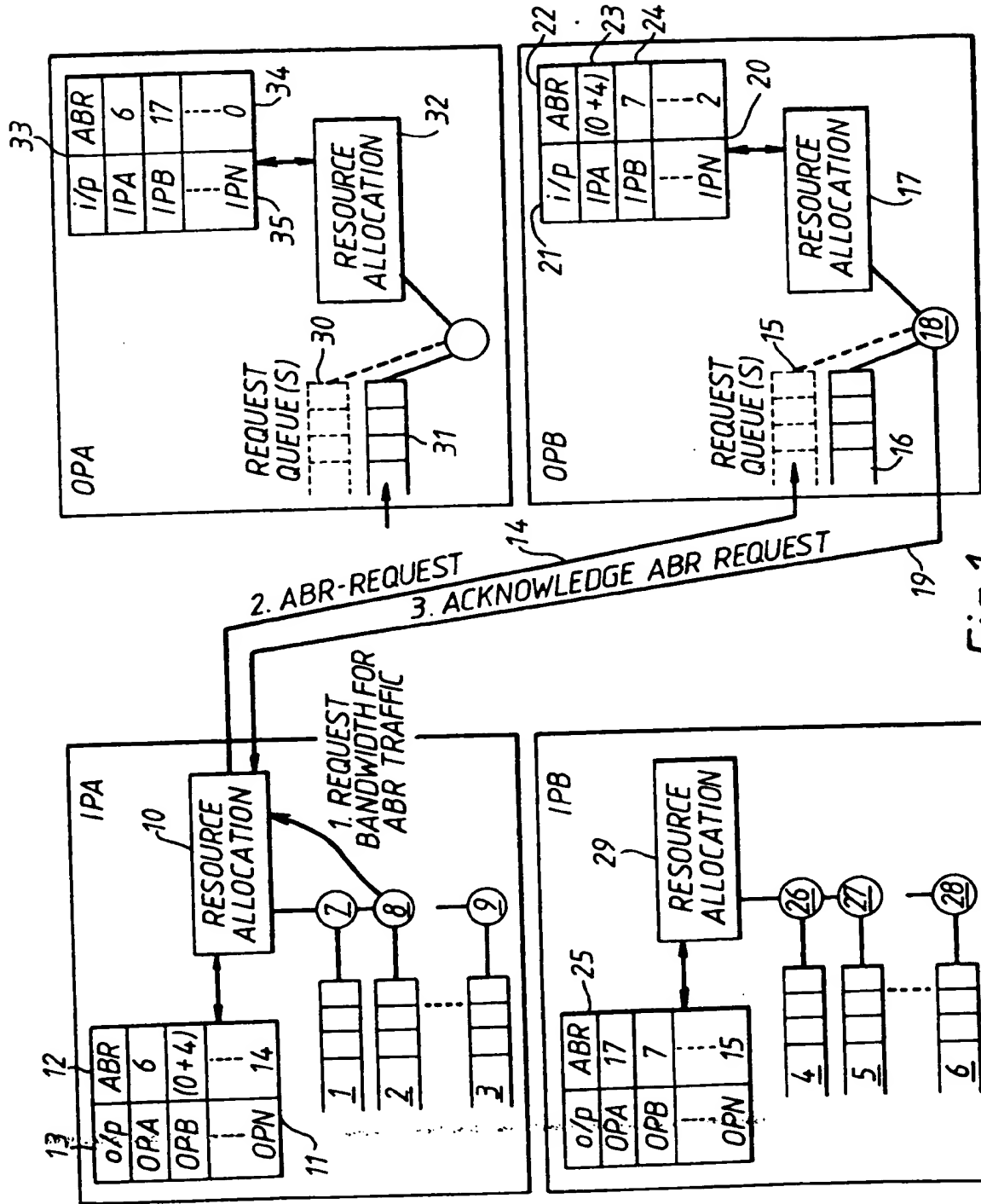
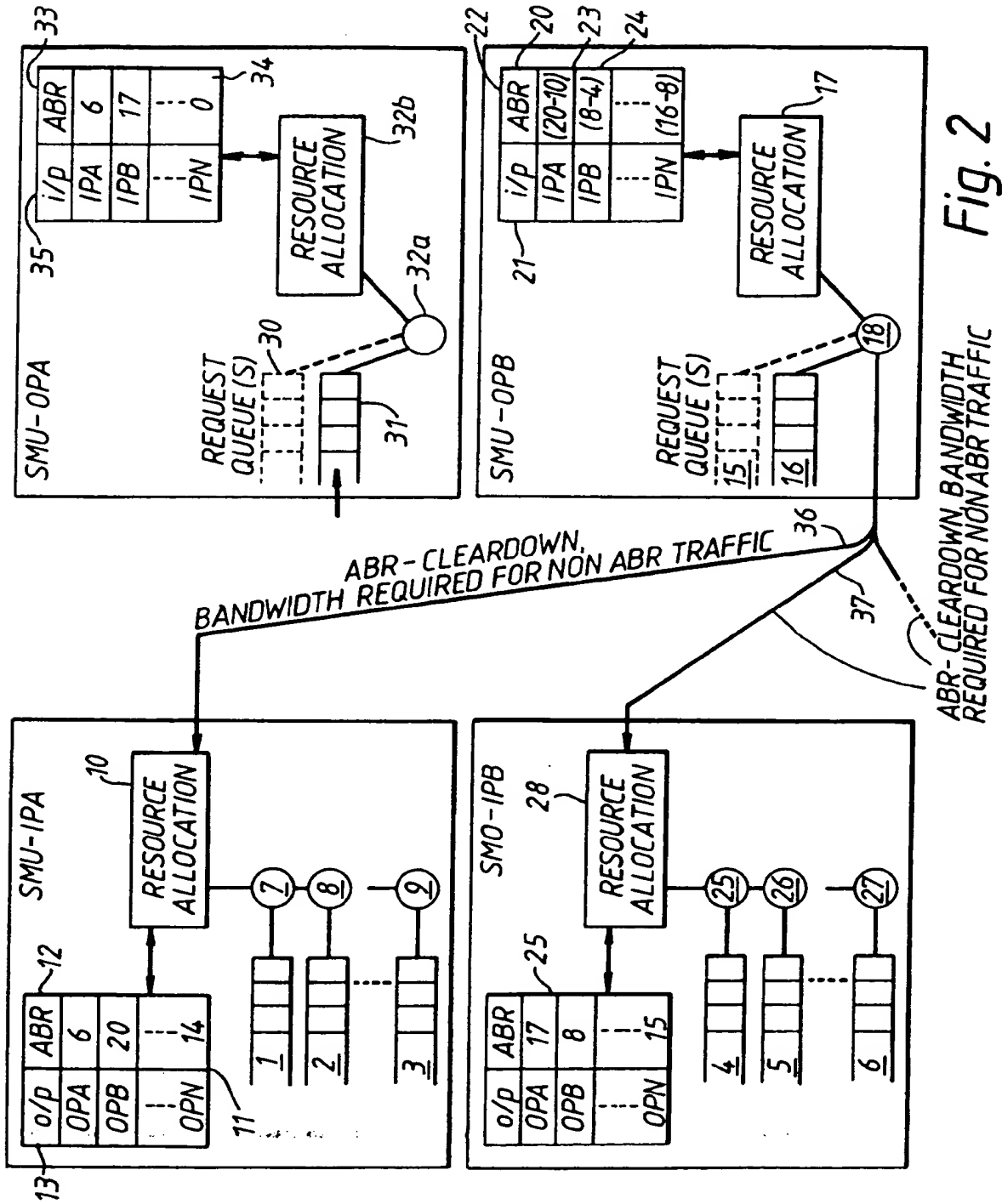


Fig. 1





European Patent  
Office

## EUROPEAN SEARCH REPORT

Application Number  
EP 95 10 4052

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	IEEE COMMUNICATIONS MAGAZINE, vol. 32, no. 3, March 1994 USA, pages 86-98, P. NEWMAN 'ATM local area networks'	1	H04L12/56
A	* page 95, left column, line 2 - line 58 *	2-5	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 37, no. 2a, February 1994 NEW YORK US, pages 243-246, 'MAC layer handling of preemptive and nonpreemptive priorities in buffer-insertion LANs' * the whole document *	1-5	
A	WO-A-86 02510 (HUGHES AIRCRAFT COMPANY) * abstract * * figure 1 *	2	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H04L
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
THE HAGUE		20 July 1995	Perez Perez, J
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			
T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EPO FORM 1500 03.92 (P04C01)

**THIS PAGE BLANK (USPTO)**